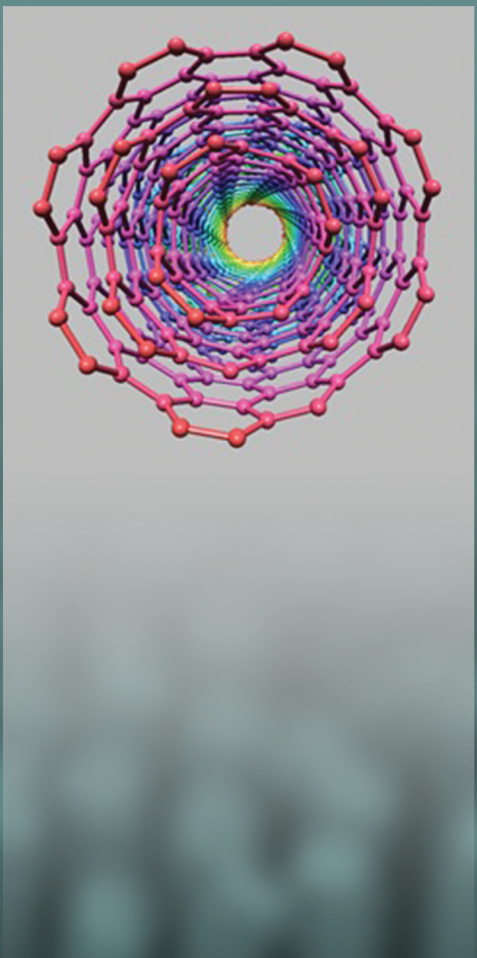
Carbon-Based Electronics

Transistors and Interconnects at the Nanoscale



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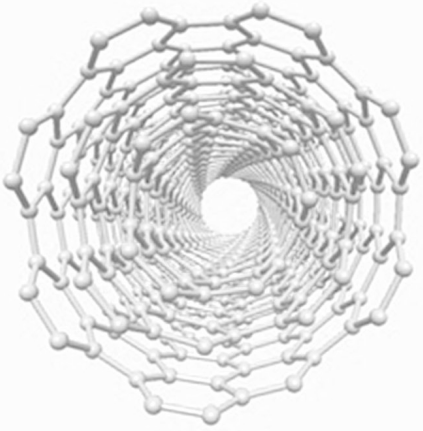

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Preface

The past 50 years have witnessed notable advancements in the field of very large scale integrated circuits with shrinking transistor geometries as predicted by Moore's law and applications in all walks of our lives. We are still guided by Moore's law. However, we are reaching the end of the curve close to year 2020 imposed by the laws of physics. Semiconductor Research Corporation in its past 2003 International Technology Roadmap ofSemiconductors report has referred to several non-classical devices, including those based on carbon nanotubes, which could be the candidates of future technology as the end of Moore's law approaches. The interconnects in sub-nanometer CMOS technology nodes are already facing problems in copper interconnect due to increase in its resistance.

Since the discovery of carbon nanotubes in 1991 by Japanese physicist Dr. Sumio Iijima, voluminous research has been done in the field of one-dimensional carbon nanotube material for numerous applications, including those for the possible replacement of silicon used in the fabrication of CMOS chips. One of the interesting features of carbon nanotube is that it can be metallic or semiconducting with a bandgap depending on its diameter. Since carbon nanotubes are planar graphene sheets wrapped into tubes, electrical characteristics vary with the tube diameter and the wrapping angle of the graphene. Carbon nanotubes can be manipulated in a controlled way in their position, shape, and orientation with the use of the atomic force microscope. Carbon nanotube as an interconnect material and its integration with CMOS process offers the much-awaited solution. In search of non-classical devices and related technologies, both the carbon nanotube–based field-effect transistors and metallic carbon nanotube interconnects are being explored extensively for emerging logic devices for very large scale integration.

Transistors in the integrated circuit design for analog, digital, mixed-signal applications, including those for radio frequency operation, require equivalent circuit models for use with device- and circuit-level simulators. Although various models for carbon nanotube–based transistors and interconnects have been proposed in the literature, an integrated approach and compatibility with present simulators are yet to be made available. This book present the material that is an attempt in this direction, where models for both transistors and interconnects based on carbon nanotubes are developed from the fundamental understanding of the material and solid-state physics and made compatible with commercial integrated circuit design simulators through Verilog-AMS codes for design and analysis of integrated circuits. A need of such an approach motivated the authors to begin developing a better understanding of current transport in metallic and semiconducting carbon nanotubes and building closed-form analytical models for the design and analysis of carbon nanotube–based integrated circuits.

An overview of single-walled, multi-walled, and bundle of single-walled carbon nanotubes, electrical properties, and carbon nanotube–based transistors, interconnection, and integrated circuit is presented in Chapter 1. In Chapter 2, current transport phenomenon in semiconducting carbon nanotubes is studied from the understanding of physics of semiconductors and closed-form analytical equations are derived. Chapter 2 serves as a basis of developing current transport model of carbon nanotube field-effect transistors in Chapter 3 similar to MOSFET models for the analysis and design of integrated circuits. The developed analytical current transport models verifying established experimental current–voltage characteristics have been used in design of basic logic gates. Integrated circuits based on carbon nanotube field-effect transistors will also need to integrate carbon nanotube metallic interconnect. In Chapter 4, a detailed study has been conducted on current transport in metallic single-walled carbon nanotubes and one-dimensional fluid model has been developed, which accounts for the electron–electron interaction, and compared with the two-dimensional fluid model. The fluid model for single-walled carbon nanotube as interconnect has been extended in Chapter 5 for multi-walled and bundle of single-walled carbon nanotubes as interconnects. Suitability of carbon nanotube, single-

walled, multi-walled, and bundle of single-walled as interconnect for ballistic transport and local and global interconnection is investigated and compared with the performance with copper as interconnects, and S-parameters are studied in detail, including the power dissipation.

Phase-locked loops are widely used in high-speed and high-frequency data communication systems. Phase noise is one of the major causes of concerns and originates mainly from one of its building blocks, the voltage-controlled oscillator, which requires high-Q inductors. Carbon nanotube wire has reduced skin effect compared to metal conductors such as the copper and has a great promise for the realization of high-Q on-chip conductors. In Chapter 6, a model of carbon nanotube as an inductor is studied, and a feasible design of a very high frequency LC voltage-controlled oscillator is presented using multi-walled and single-walled bundle wires as an inductor in the LC tank circuit. The observed reduced phase noise in voltage-controlled oscillator makes the high-Q carbon nanotube wire inductors a very promising component for RF circuit design. Energy recovery techniques are playing an important role in modern electronic circuit design due to urgent need of low power dissipation in portable communication and computing systems. Although energy recovery techniques for CMOS circuits are well developed, such techniques are not fully explored for carbon nanotube field-effect transistor–based circuits. In Chapter 7, we have explored design and analysis of basic energy recovery carbon nanotube field-effect transistor circuits based on models developed in Chapter 3 and CMOS-based energy recovery design styles. We have shown that much work is needed to reduce the on-chip power density above 1 GHz. While developing current transport models for transistors and interconnects based on carbon nanotubes for integrated circuit design, it was observed that the compatibility of models with simulator such as SPICE is too difficult and time consuming due to the complexity of models. Instead, Verilog Analog Mixed-Signal (Verilog/AMS) solves the much complex problem and fewer steps are required for simulations. This is because model equations for new devices can be put into the Verilog-AMS coding and simulator will call the code. Chapter 8, the last chapter, concludes with Verilog/AMS codes for the carbon nanotube field-effect transistor in Cadence and usefulness demonstrated.

This book can serve as a textbook for graduate-level course in nanoelectronics for students in electrical and electronics engineering, applied physics, and materials science with focus on reduced-dimension materials such as carbon nanotubes. The material covered in the book will be very useful for graduate students for thesis and dissertation research exploring the integration of carbon nanotubes as interconnects with sub-nanometer CMOS technology nodes, high-frequency and high-speed electronics, carbon nanotube field-effect transistor sensor electronics, and numerous other applications. The book will be very useful for practicing engineers in the field of VLSI design and technology, semiconductors, nanoscience and nanotechnology, and microelectronics.

The authors would like to thank Drs. Yang Liu and Rajiv Soundararajan for the design and testing of carbon nanotube–based integrated circuits in Cadence using developed models for field-effect transistors and wire inductors. The authors gratefully acknowledge Mr. Clay Mayberry of the United States Air Force Research Laboratory, New Mexico for his strong support, encouragement, and useful discussions. The book would have not been complete without the encouragement and support of our families. We would like to give special thanks to our families: to my wife, Shashi, son, Siddharth, daughter, Gitanjali, son-in-law, Saurabh, grandson, baby Ayaan, and my old mother back in India for their continued support and encouragement (Srivastava); to my parents and sisters for their constant encouragement and support (Marulanda); to my wife and sons for their support (Xu); and my daughter, Anna, son, Andrei, and my father, Mohinder, for their support and encouragement during the course of the writing of the book (Sharma).

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