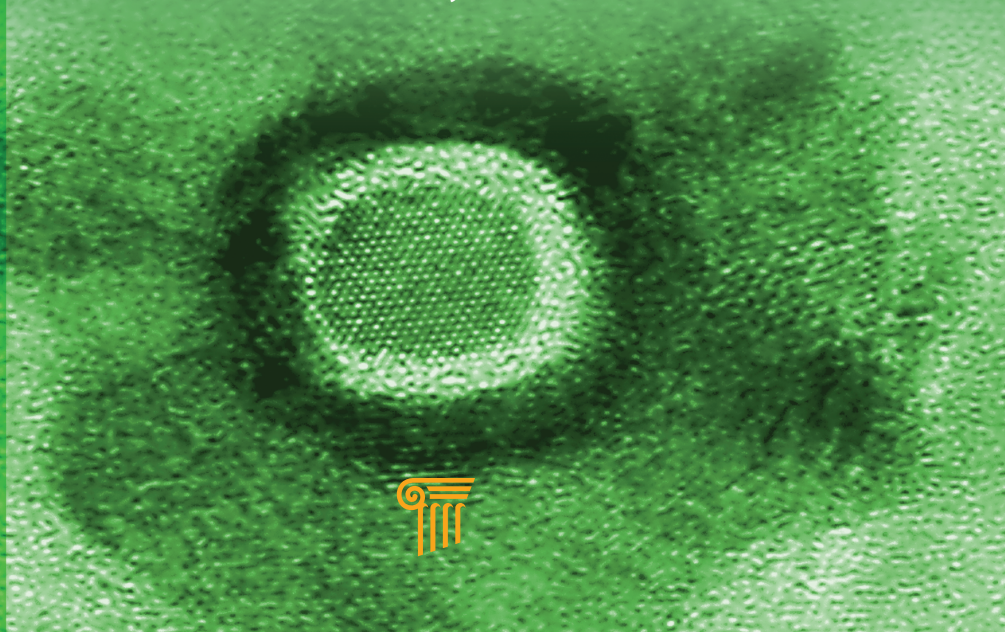
Pan Stanford Series on Intelligent Nanosystems Volume 1

INTELLIGENT INTEGRATED SYSTEMS

Devices, Technologies, and Architectures

edited by Simon Deleonibus



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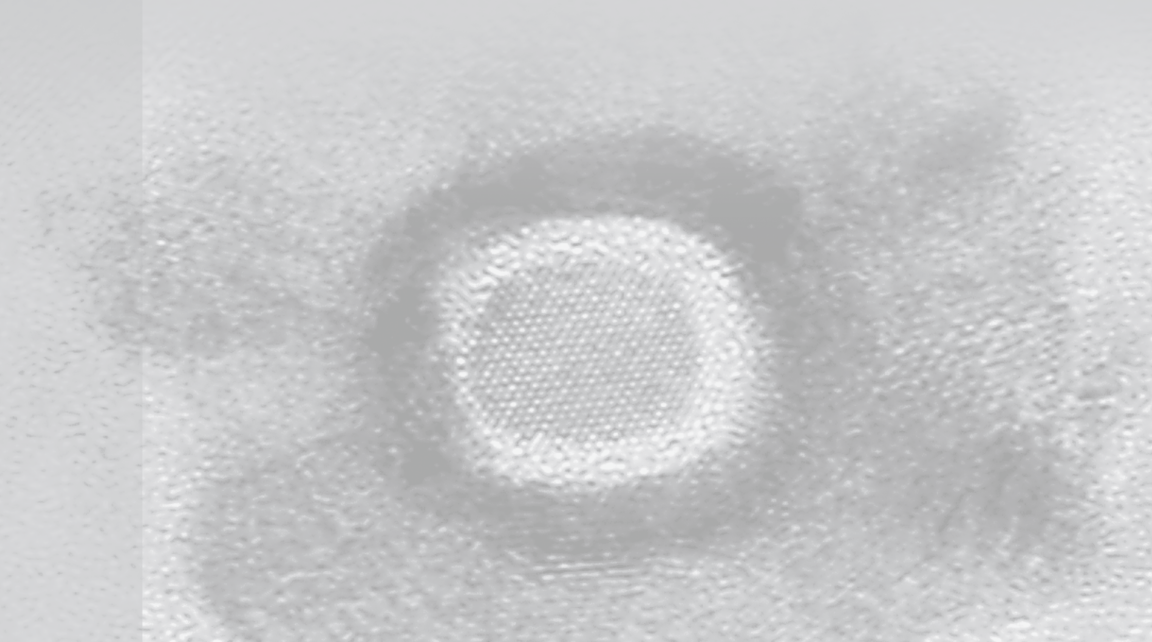

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PAN STANFORD PUBLISHING

Published by

Pan Stanford Publishing Pte. Ltd.
Penthouse Level, Suntec Tower 3
8 Temasek Boulevard
Singapore 038988

Email: editorial@panstanford.com
Web: www.panstanford.com

British Library Cataloguing-in-Publication Data
A catalogue record for this book is available from the British Library.

Intelligent Integrated Systems: Devices, Technologies, and Architectures

ISBN 978-981-4411-42-4 (Hardcover)
ISBN 978-981-4411-43-1 (eBook)

Printed in the USA

Contents

Acknowledgements

I wish to congratulate all co-authors of the fourteen chapters of *Intelligent Integrated Systems: Devices, Technologies, and Architectures* for the results of their brilliant research as well as for writing excellent contributions including a review of the state of the art in their respective fields. They are worldwide recognized researchers and belong to top-level renowned universities and institutes. Their faith and efforts were key in making this ambitious project a success.

It is an honor to receive support for the book's promotion from Prof. Hiroshi Iwai of Tokyo Institute of Technology (Yokohama, Japan), Prof. Tso-Ping Ma of Yale University and Prof. Mikael Ostling of KTH (Kista, Sweden). Their influence in the nanoelectronics, nanotechnology and nanoscience world distinguishes the scientific level of the different contributions.

I have special thanks to address to Mr. Stanford Chong, Mr. Sarabjeet Garcha and the staff of Pan Stanford Publishing for being available throughout the publishing process from the definition of the book content to the preparation of final edition and the promotion of this book.

Finally, none of this would have been possible without the moral support and patience of my wife Geneviève and my son Tristan. Their dedicated attention has been of first importance to me. I wish to dedicate this work to them.

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Introduction

Intelligent Integrated Systems Forward to Zero Variability and Zero Power!

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Since its invention, the integrated circuit technology has allowed to put on the same piece of semiconductor from a few working devices, at its very beginning, to tens of billions nowadays. The increasing complexity of integrated circuits qualifies them as intelligent nanosystems. The Pan Stanford Series on Intelligent Nanosystems will include several books aiming at reviewing all aspects of active and passive device physics, their technology, and device to system architectures.

In this book, which is the first in the series, we review the state of the art of intelligent integrated systems device technology and architectures through the new critical modules that could enhance CMOS performance or reduce power consumption, new devices architectures, added functions by bringing in new memory devices: molecular memories, resistive memories possibly leading to neuromimetic devices and architectures, nanoelectromechanical systems, smart microelectromechanical systems, and 3D wafer-level packaging. Various critical aspects to downscale CMOS devices are

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ISBN 978-981-4411-42-4 (Hardcover), 978-981-4411-43-1 (eBook)
www.panstanford.com

covered, such as metallic Schottky source and drains, thermal body behaviour by the use of diamond, new channel materials such as germanium, III–V and carbon materials (CNTs, graphene). Carbon-based materials are considered for interconnect, potentially alleviating the issue of electromigration in high aspect ratio vias. Tunnel field-effect transistors are reviewed as a serious candidate for ultra-low supply voltages less than 0.5 V. 3D monolithic integration would for sure be a good way to integrate new materials at a front-end level and obtain the highest packing density. Meanwhile, stacked parallel 3D is another way to increase the number of functions at the level of a system, allowing consequently heterogeneous integration and its packaging strategy. In many aspects and because of the adoption of the technologies for nomadic, portable, and handheld usages, quasi zero power and quasi zero variability will be a future challenge and necessity for their success at the sub-5-nm level. At this level, molecular dimension fluctuations will induce dramatic variations of device characteristics. New paradigms will be necessary to fabricate devices and circuits, using quasi zero intrinsic variability processes. The manipulation of monodisperse objects like molecules, nanoparticles and nanocrystals could need to be mastered in possible self-assembled schemes. This subject will be reviewed in the second book of the Series on Intelligent Integrated Systems.

I.1 Scaling and Diversifications

The history of microelectronics is a succession of events that most people wouldn't have dreamed of 50 years ago: it was the common thought among the population at that time, when only few people would have expected the amazing impact of electronics and, further on, integrated circuits technology, on our way of life. Thanks to the scaling of device dimensions in the past 55 years, humanity has experienced the most impressive progression of technology in its history impacting and somewhat reshaping all aspects of our daily life. Microelectronics is a pervasive technology which enables an increasing number of functions and services that our societies evolutions are based on.

I.1.1 *Moore's Law as an Archetype Progress Law for Microelectronics*

Moore's law represents the reference for the evolution of microelectronics progress. By stating that the number of devices on a chip would double every year [1], Gordon Moore made the first prediction of microelectronics progress. In order to make it practical, a scaling theory was necessary, whereas miniaturization of devices has been proven to be the inevitable path [2, 3]. To date in 2012, since the invention of the first integrated circuit [4], the number of devices on a chip has been multiplied by 10 orders of magnitude. This is an unprecedented performance that an art, skill or technology has ever made in the history of humankind. The progress is such that the calculation capacity each human being holds in his hands today is 10^{10} times larger than in 1946 with the first ENIAC, at a time when only a small group of people had the possibility to manipulate a calculator or a computer! Only few people believed and predicted the fantastic evolution of PCs or the cellular phone market. The scaling of CMOS devices and their fabrication, thanks to silicon technologies, made it available and possible.

The evolution of microelectronics into the nanoelectronics world is mainly due to a "technology-push"-based progress. Scaling is still relevant as long as power consumption and speed can be improved with a minimum variability and highest cost-effectiveness. Technical hurdles appear and request international cooperation between competitors of different profiles, such as research institutes, universities, fabless companies, equipment suppliers, integrated device manufacturers and foundries, acting on the whole value chain of the semiconductor business. A typical outcome of these collaborations is the International Technology Roadmap of Semiconductors [5]. The increasing cost of R&D, which was seen as a limit for further development, is finally alleviated by sharing the burden in the frame of consortia [6], affiliate research programs [7] and various types of agreements with partners on the basis of win-win principles [8]. Among the questions that international consortia will have to address in the next years, variability, in relation with a large number of components and their characteristic statistical distribution due to their size, is among the biggest ones.

The next great challenge for nanoelectronics will be to make massively available, to the worldwide population, ultra-low-power and high-performance devices and systems.

Devices and systems that consume quasi zero power in standby and deliver high performance with a low power–delay product when active will be necessary to develop autonomous, heterogeneous integrated systems at low cost. This will give access to advanced technologies to a large number of people on the planet with energy saving, sustainability and large mobility capabilities. In that frame, integrated circuit technologies based on fully depleted devices (in their FDSOI, FinFET, Trigate versions) are a good and necessary first step. Further on, device scaling and the preservation of high mobility will impose ultra-low-voltage power supply. Tunnel field-effect transistors will be a major architecture option to build extremely low-power-consuming devices. These devices can be made by building a thin-film-channel-based architecture. The physical limits of silicon CMOS scaling open the question of alternative materials to silicon channels as possible new candidates. However, silicon is still the main stream for ultra-highly scaled CMOS and is foreseen as the main base material for active devices by the end of the roadmap and beyond [5]. These materials can be co–integrated as thin films with silicon devices thanks to low-temperature wafer bonding [9].

I.1.2 *Benchmarking Several Possible Channel Materials*

The question of channel materials alternative to silicon is being debated since silicon has been introduced to make microelectronic devices. Table I.1 reports some important physical features of different materials that have been proposed to challenge silicon (see also [10]). The success of silicon is mainly due to its use in obtaining high-quality dielectric SiO_2 by thermal oxidation, not to its highest low field mobility. Still, low field mobility is not the only parameter to be taken into account when a device architecture is being optimized.

The saturation velocity is a very important feature to know if analog, high-frequency and digital performances are expected. As a matter of fact, one can see that InGaAs and GaAs have lower saturation velocity than silicon, whereas the low mobility

Table I.1 Physical characteristics of semiconducting Column IV materials and III–V compounds (see also [10])

Material	μ_n ($cm^2\ V^{-1}s^{-1}$)	μ_p ($cm^2\ V^{-1}s^{-1}$)	s_{th} (W/m/K)	Rel. K	Eg(eV)	$v_{sat}(10^7 cm/s)$	$ni(cm^{-3})\ (m^*_e m^*_h/m^2)\ T^{1/2}$ $exp(-Eg/2kT)$
Si	1400	500	141	11.9	1.12	0.86	2×10^{10}
Ge	3900	1900	59.9	16	0.66	0.60	2×10^{13}
GaAs	8500	400	55	12.9	1.42	0.72	2.1×10^{6}
$InGa_{0.47}As_{0.53}$	12000	300	5	13.9	0.74	0.6	6×10^{11}
InSb	77000	850	1.8	16.9	0.17	5.0 @ 77K	2×10^{16}
C-Diamond sp^3	2200	1800	2000	5.7	5.47	2.7	10^{-27}
Graphene (CNT) sp^2	10^4–10^5	10^4–10^5	1000	5.7	Semi-metal	4	$1 \times 10^{12}\ cm^{-2}$ (1×10^{15})

is far better in III–V materials. Unfortunately, "dark space" is expected to be larger in III–Vs than in silicon, which reduces their possibility of scalability for low-power applications compared to silicon [11].

However, if a compact design layout is needed, as in a CMOS SRAM memory cell or an elementary CMOS inverter, then the ratio of low field electron to hole mobilities, μ_n/μ_p, needs to be as close as possible to 1. From Table I.1, one can see that the layout of a CMOS SRAM cell would have a lower density with InSb as a channel material than with silicon. Among the candidates listed in Table I.1, carbon-based materials would be the best choice to obtain the best layout density for a given function. Equal hole and electron mobilities are possible in sp^2 carbon-based materials (C-diamond [10, 12], CNT [13], graphene [14, 15]). In these latter examples, carriers are expected to be balistic or emitted in resonant modes into the MOSFET channel. Unfortunately, their low or almost zero bandgap is a handicap to compete for low standby power CMOS applications. However, by using p–i–n FETs architectures, band-to-band tunneling operating mode MOSFETs with less than 60 mV/dec subthreshold swing have been demonstrated possible [13].

Dopant activation in carbon materials is still limited [16] despite the fact that progress has been made for p doping in diamond by the end of 1990s [17]: however, ohmic contacts of metal to diamond need to be optimized. Moreover, C-diamond is the highest thermal conducting material (10 times the thermal conductivity of silicon or 50 times the thermal conductivity of Al_2O_3) [18] and could be integrated as a buried layer to suppress self-heating or introduce a thermal equalizer in future semiconductor-on-insulator substrates [10, 12]. The dielectric constant of C-diamond ($K_C = 5.7$) as a buried layer would offer the best trade-off between HiK and SiO_2 to control short-channel effect and DIBL [10].

In the future, heterogeneous co-integration will be possible by the use of in-line thin-film bonding and subsequent processing. Thanks to the possibility of processing these films at low temperatures, the use of 3D integration will be one way to heterogeneously co-integrate several materials while keeping quasi-optimized devices characteristics [10, 19–21].

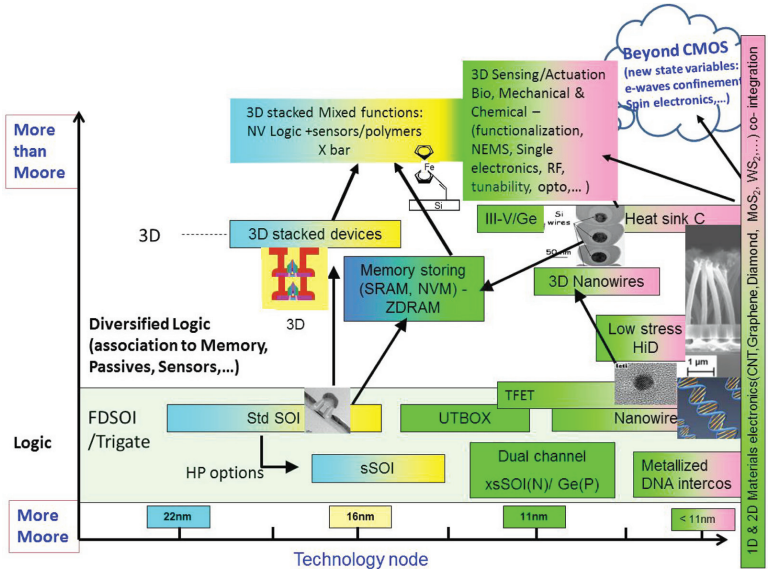

Figure I.1 Vision of a unified platform on SOI, including heterogeneous More Moore, More than Moore and Beyond CMOS types of devices.

Thanks to the use of wafer bonding and cold end processing, many opportunities to mix More Moore, More than Moore and Beyond CMOS types of devices for new functionalities and applications will show up. Figure I.1 gives an example of what can be achieved at the front-end level based on the integration of active (for channels) and passive thin films. Thanks to thin-film-based technology and the necessary evolution towards cold end processing, it will be possible to co-integrate and stack devices delivering different functionalities and possibly using different active materials. Many of the materials appearing as examples and opportunities in Fig. I.1 will be co-integrated with silicon thanks to low-temperature processing. As typical examples, in a sequential integration second strata Si, Ge and III–V channels will require low-temperature dopant activation and diffusion. Furthermore, polymers linking to silicon and back end of line metals would require to maintain the end of process temperatures lower than metal alloying temperatures. The integration of carbon-based materials (carbon nanotubes, graphene,

diamond, etc.) is a serious option for multifunctional applications as well as low resistivity, high resistance to electromigration long interconnect and vias. These materials exhibit high thermal conductivity, which should contribute to lowering heat dissipation and hot spots in a circuit.

Thanks to the new flexibility offered by low-temperature processing, new associations between logic and memory devices will thus be possible in the field of non-volatile logic, power management, functions and circuit re-configurability, neuromimetic architectures, and so on. The various options which are shown to be possibly co-integrating (in Fig. I.1) are reviewed in this volume. It will be possible to add or associate stand-alone devices such as smart sensors or other circuits. 3D wafer-level packaging is a serious option to optimize the packing density of the final systems.

These new possibilities, which will be accessible thanks to the technological progress, will be achieved in parallel with scaling of nanoelectronic devices. The choice of the device architecture materials and process integration options will be done under the light of minimal variability as long as the critical size of the devices and interconnect is far from molecular size. However, at the sub-10-nm level, the control of the intrinsic part of variability depending on the specific process step characteristics will become a major issue.

Statistical variability has a double nature: some causes are *intrinsic*, depending on the basic principles of the fabrication process conception; other causes are *extrinsic*, due to the ultimate performance of the equipments and process integration. Ultra-scaled sub-5-nm devices and interconnect will request the control of quasi zero variability technologies. At this level, molecular dimension fluctuations will induce dramatic variations of device characteristics. New paradigms will be necessary to fabricate devices and circuits, using quasi zero intrinsic variability processes. The manipulation of monodisperse objects such as a discrete number of molecules, nanoparticles and nanocrystals and process control at the atomic level will need to be mastered in possible self-assembled schemes. This subject will be reviewed in the second book of the Series on Intelligent Integrated Systems.

I.1.3 *New Progress Laws and Paradigms*

Moore's law could temporarily be slowed down because of the major showstoppers encountered by CMOS physical limitations and the cost of lithography [5]. The strong demand for an increasing number of functions by the use of nomadic handheld objects is motivating research and development on diversification, heterogeneous integration and 3D packaging. Miniaturization, as a progress law, is well adapted to the increase of the number of devices per chip at a reduced cost per function, reduced power consumption and increased speed. In the More than Moore domain, miniaturization does not necessarily bring an improvement of the single devices' figures of merit (F.O.M.). However, miniaturization can be relevant to access highly resolved sensing, reduce the cost, and make the systems available to a larger public.

Intelligent integrated systems will be massively available in the future thanks to the high level of integration and the associated reduced cost brought by miniaturization and heterogeneous co-integration of sensors and actuators as well as passive and active devices. Multiphysics data and physical quantities will be processed or even fusioned with other data of a different nature [22] to deliver new resultant functions and the possibility to decision making. The mimetism of human senses is one of the archetype examples which are still very challenging today. The association of the different senses' imitation combined with data fusion could result in augmented systems as compared to the human body's functions and give rise to new applications (Fig. I.2).

Miniaturization is one practical approach to Moore's law: it is economically efficient whenever it is realized in the frame of collective fabrication. However, the physical limits of transistor scaling and the cost of investments inspires researchers to envisage new paradigms such as device or circuit stacking in 3D scheme integration. The 3D stacking or packaging approach can potentially increase the number of devices per chip or improve the performance of a system rather than relying exclusively on scaling. Microsystems can profit by the evolution of microelectronics to follow the miniaturization scheme. Some figures of merit, such as the resolution of MEMS, can be improved by making devices smaller.

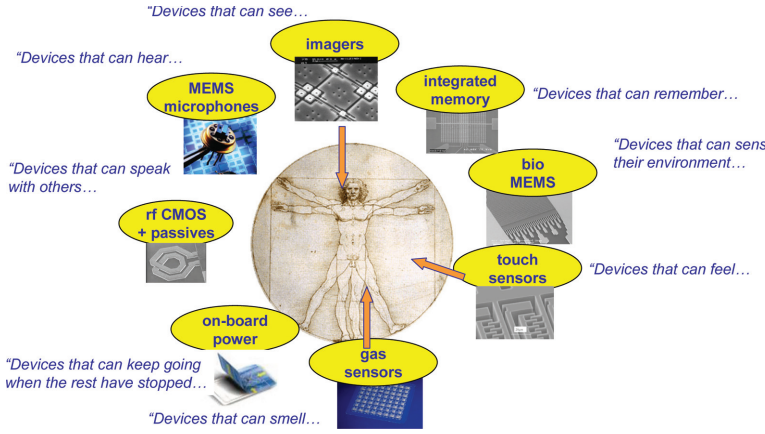

Figure I.2 Analogy between senses and electronic, micromechanic, and magnetic device sensors. The association of the different senses' mimetics will give rise to new applications: data fusion will then be welcome to make these new applications easy.

Their sensitivity can be upgraded when gravimetric properties are exploited [23]. However, their cross sections get smaller as well and reduce the interaction probability with any object of a comparable size. The integration of multiple devices taking advantage of collective fabrication and the resolution of lithography coming from microelectronics can bring a solution to that issue. That is the case for nanoelectromechanical system (NEMS) resonators arrays, which increase their responsivity by increasing their capture area. Consequently, the improvement of the figures of merit of NEMS devices integrated on silicon is not necessarily obtained by their scaling. The progress in heterogeneous co-integration is thus to be considered through new progress laws which will mainly require taking into account the application area specifications.

I.2 Intelligent Integrated Systems: Device Technologies and Architectures

In this book, we highlight the different technologies that will bring future intelligent integrated systems into reality. We have

selected timely topics in the fields of technology and architecture and organized them into two sections. In section 1, we review in eight chapters the various option for advanced silicon-based CMOS. New materials and device architectures are studied as possible candidates to sustain the scaling of CMOS. Section 2 reports in six chapters (Chapters 9 to 14) the new paths to augmented silicon-based technologies. New functions will be enabled by the heterogeneous co-integration of resistive memories using organic molecule grafting on silicon, oxygen vacancies diffusion in metallic oxides, or spin transfer associated with a nonlinear device (transistor or diode). Programmable neuromorphic devices and architectures will be possible by these associations. Power management as well will profit by the availability of their integration. 3D integration in different flavours is developed as one of the most preferred options for these new functional assemblies. These schemes will, furthermore, be used more and more in the future in the co-integration of sensors with digital or analog integrated electronics. It will be a very good way to minimize power consumption, signal-to-noise ratio, and speed. Ultra-miniaturized resonators that use nanowires are a good example of NEMS which will benefit from nanoelectronic integration and co-integration capabilities.

Intrinsic statistical variability is nowadays already guiding the device architecture choice for sub-28-nm nodes. Several solutions have been proposed at the system design and components architecture level. In Chapter 1, Andrieu et al. demonstrate the capabilities of thin-film channel CMOS devices in order to drastically reduce their variability due to random dopant fluctuations. The potentialities of planar, trigate, and nanowires to fulfill the requirements are reviewed. Today, fully depleted devices architectures are introduced into production by several companies at the sub-22-nm technology node as defined by the ITRS [5].

The access resistance to channel MOSFET is more and more limited by the source and drain resistance as these electrodes need to be scaled with MOSFETs. In Chapter 2, Dubois et al. give the status of the recent developments in low-temperature dopant-segregated Schottky barrier MOSFETs. Introducing metallic access electrodes to the channel together with a doped contact which allows reducing

the contact resistance is a very popular strategy that excites many researchers worldwide.

In Chapter 3, Mazellier et al. report on a silicon-on-diamond (SOD) substrate technology, in which diamond replaces buried silicon dioxide used in conventional silicon-on-insulator (SOI) wafers. Diamond is interesting because of its high thermal conductivity (compared to SiO_2) while maintaining high resistivity (electrostatic control). SOD technology is thus ideally suited for SOI applications requiring enhanced thermal management, potentially high-speed 3D complex systems. Diamond can be efficiently integrated in a thin-film configuration and leads to significant improvement in heat dissipation.

In Chapter 4, Le Royer et al. give the status on the process of advanced substrate wafers based on SGOI (SiGe alloy film on insulator) and GeOI (germanium on insulator) and innovative device integration. Various realization schemes are demonstrated for the substrate fabrication such as Ge enrichment, Smart-Cut™, and hybrid epitaxial growth. Fully depleted CMOS, impact ionization MOSFETs and tunnel FETs have successfully been co-integrated on the obtained state-of-the-art substrates whereas germanium on insulator offers the opportunity to exploit theses novel architectures.

In contrast with parallel or back-end 3D integration in which the layers are processed independently on separate wafers and bonded to each other after device and BEOL fabrication, 3D monolithic integration stacks the layers sequentially on top of each other. In Chapter 5, Vinet et al. demonstrate that this approach, different from parallel 3D by its front-end type nature, offers new design opportunities based on electrostatic coupling and gain in density to boost the performance. 3D monolithic integration allows to reduce circuit area by 40% compared with conventional layout and delay.

Another way to increase performance different from scaling is to bring in new transistor channel materials. This option is reviewed in Chapter 6 by Datta on the contribution from III–V and in Chapter 7 by Li et al. on carbon electronics. Compound semiconductor- or III–V-based quantum-well field-effect transistors (QWFETs) or heterostructure field-effect transistors (HFETs) are a promising transistor architecture option for future ultra low power/high speed logic applications (Chapter 6). In Chapter 7,

the authors add the opportunities to integrate carbon-based interconnect to carbon-based active devices channels. The physics of carbon-based materials is overviewed in this chapter and the opportunities for new applications are highlighted. This is for sure an open new field for fabrication and new functional device architectures for high-frequency MOSFETs, TFETs, spin electronics, as well as superior quality behavior passive components, despite the remaining controversial issues for these materials integration.

Knoch focuses on tunnel field-effect transistors in Chapter 8. The hope to be able to reduce the subthreshold swing of MOSFET-type devices to values lower than 60 mV/dec has been demonstrated by several authors in the past 10 years, but the optimal drivability has not yet been obtained. Professor Knoch has made undoubtedly major developments on TFET technology as well as their physics: the challenges to realize optimized heterostructure TFETs compatible with applications are explained in this chapter.

Adding new functions to nanoelectronics or finding new paths is a constant quest of interest as long as low-cost applications can be defined. Memories are very useful to define the various functions in a system. In Chapter 9, Buckley et al. show the opportunity to use memories employing organic-based molecular or polymer layers. Such technologies explore the use of low-cost "bottom-up" approaches (i.e., chemical synthesis, surface functionalization, molecular self-assembly): they may have some features of interest to mainstream storage technologies within the next few decades, and on a shorter term address new markets (plastic electronics, flexible/wearable electronics, etc.).

Chapter 10, by Magyari-Köpe and Nishi, is dedicated to non-volatile resistive switching memories (RRAMs). The RRAM is built as a MIM capacitor–like structure where the insulator layer (I) is made of one of two kinds of materials, transition metal oxides or solid-state electrolytes. Progresses in materials and device structures of RRAMs are reviewed with certain emphasis on physical mechanisms for resistive switching and also electronic conduction in the low resistance state for different insulators and metal electrode materials. The mixing of these devices with CMOS can open the way to new applications such as neuromorphic computing.

The pervasion of nanowire technology is illustrated in Chapter 11 by Duraffourg and Ernst: applications which differ from scaling of transistors have been developed in the field of sensors. A technical overview of suspended silicon nanowires used as high-frequency (HF) vibrating NEMS is given. Among the various applications which can be addressed with such nanosystems, nanowires represent the HF nanoresonators for future ultra-low-mass sensors.

Among the new emerging fields, spintronics is a combination of magnetism and microelectronics. Magnetic tunnel junction resistance depends on the junctions' magnetic configuration (magnetoresistance), which can be used to store information. They combine nonvolatility with hardness to radiations, low-power consumption, speed, density, and quasi-infinite endurance: they may thus replace parts of the memory hierarchy and allow conceiving a normally-OFF/instant-ON low-power electronics (More than Moore). In Chapter 12, Prenat et al. describe spintronic phenomena, technology, and devices as well as their use in memory, logic, and RF applications. This is a way to add new functionalities to microelectronics.

Besides adding new devices such as sensors to microelectronics, as illustrated in Chapter 11, one can add intelligence to stand-alone sensors to interface signal processing and actuation electronics. In Chapter 13, Esashi reviews major examples of sensors fabricated on the basis of MEMS technology: capacitive pressure sensors fabricated by wafer-level packaging, electrostatically levitated rotational gyroscopes developed for high-precision inertia measurement systems, tactile sensor networks driven by event for safe nursing robots, acoustic sensors for wireless sensing, optical scanner for 3D imaging, sensors at the end of catheter in blood vessel, and microprobes with high spatial resolution and high sensitivity.

Finally, the devices and circuits made from the above-mentioned technologies would not be usable if their packaging weren't taken into consideration. In Chapter 14, Poupon points out the two categories of systems that nanoelectronics, in its evolution to offer more and more functions, will be handling in the future: system in package (SiP), assembling several components into one package, and system on chip (SOC), integrating functionalities at a level close to core CMOS. In SiP, different technologies are used to meet specific

needs: one of the most promising approach to meet them is 3D parallel integration. This technology involves several developments, including stacked devices or packages, silicon interposer with through silicon vias, and embedded technologies.

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