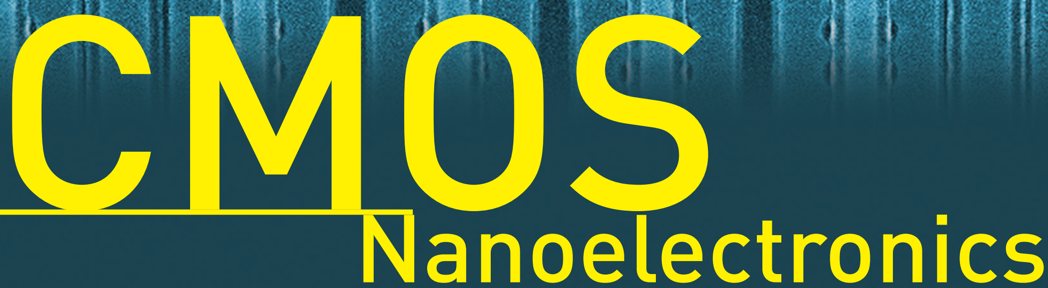
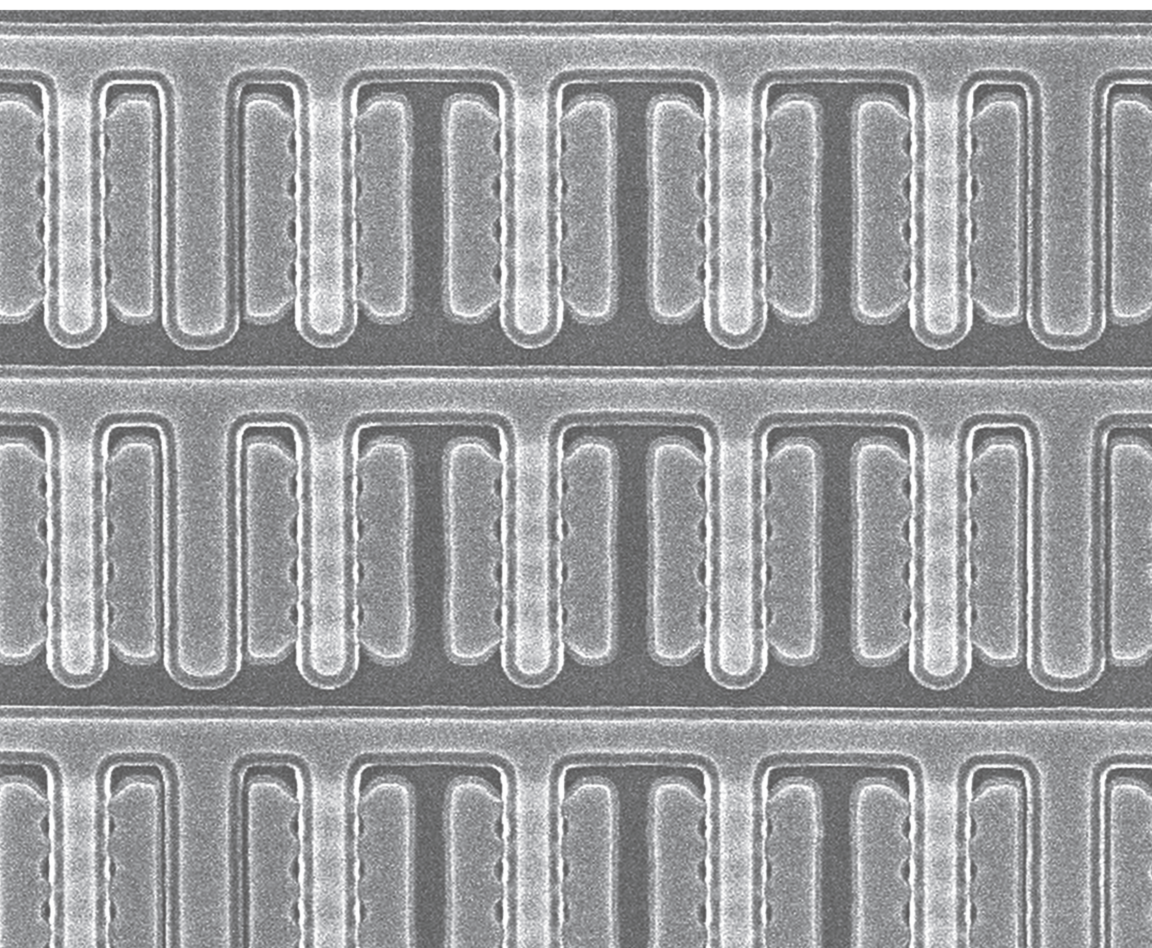


CMOS Nanoelectronics

INNOVATIVE DEVICES, ARCHITECTURES, AND APPLICATIONS

edited by
Nadine Collaert

CMOS
Nanoelectronics



CMOS Nanoelectronics

INNOVATIVE DEVICES,

ARCHITECTURES,

AND APPLICATIONS

edited by
Nadine Collaert

PAN STANFORD PUBLISHING

Published by

Pan Stanford Publishing Pte. Ltd.
Penthouse Level, Suntec Tower 3
8 Temasek Boulevard
Singapore 038988

Email: editorial@panstanford.com
Web: www.panstanford.com

British Library Cataloguing-in-Publication Data
A catalogue record for this book is available from the British Library.

CMOS Nanoelectronics: Innovative Devices, Architectures, and Applications

Copyright © 2013 Pan Stanford Publishing Pte. Ltd.

All rights reserved. This book, or parts thereof, may not be reproduced in any form or by any means, electronic or mechanical, including photocopying, recording or any information storage and retrieval system now known or to be invented, without written permission from the publisher.

For photocopying of material in this volume, please pay a copying fee through the Copyright Clearance Center, Inc., 222 Rosewood Drive, Danvers, MA 01923, USA. In this case permission to photocopy is not required from the publisher.

ISBN 978-981-4364-02-7 (Hardcover)
ISBN 978-981-4364-03-4 (eBook)

Printed in the USA

Contents

Preface xv

I. Integration of Multi-Gate Devices (FinFET)

1 Introduction to Multi-Gate Devices and Integration Challenges 3
Nadine Collaert
1.1 Introduction 3
1.2 It Is All in the Lambda … 5
1.2.1 Where do These Short-Channel Effects Come From? 6
1.3 SOI MuGFET Versus Bulk MuGFET 9
1.4 A Typical MuGFET Process Flow 11
1.4.1 Challenges 12
1.4.1.1 Fin width patterning 12
1.4.1.2 Work function engineering 15
1.4.1.3 Access resistance 17
1.4.1.4 Strain engineering 19
1.5 From MuGFET to Nanowires 21
1.6 Conclusions 22

2 Dry Etching Patterning Requirements for Multi-Gate Devices 29
Efraín Altamirano-Sánchez, Tom Vandeweyer, and Werner Boullart
2.1 Introduction 29
2.2 Fin Patterning Strategy 32
2.2.1 Patterning Stack 33
2.3 Fin Patterning: Dry Etching Process Development 35

2.3.1 Process for Fin Patterning on a Multi-Gate Architecture (193 nm Lithography) 35
2.3.2 Process for Fin Patterning with a 90 nm Fin Pitch for a 22 nm Node 6T-SRAM Cell (193i) 38
2.3.2.1 Fin critical dimension control 41
2.3.2.2 Control of the sidewall roughness 42
2.3.2.3 Fin profile optimization 46
2.3.3 Process for Fin Patterning for a Sub-22 nm and 16 nm Node 6T-SRAM Cell (EUVL) 50

3 High-*k* Dielectrics and Metal Gate Electrodes on SOI MuGFETs 57
Isabelle Ferain
3.1 Gate Electrodes in MuGFETs 58
3.1.1 ITRS Requirements 58
3.1.2 Metal Gates for MuGFETs 60
3.1.2.1 MOCVD TiN 62
3.1.2.2 ALD TiN 64
3.1.2.3 PE-ALD TiN 65
3.1.3 Gate Stack Processing 66
3.1.3.1 Pattern transfer 66
3.1.3.2 Polysilicon patterning 66
3.1.3.3 Hard mask removal 68
3.1.3.4 Metal Gate patterning 69
3.1.4 Polysilicon Corrosion 69
3.1.4.1 Polysilicon corrosion enhancing factors 70
3.1.4.2 Impact on device scalability 71
3.1.4.3 Impact on threshold voltage 72
3.2 Multiple-V_T Implementation 74
3.2.1 Introduction 74
3.2.2 Channel Modification 77
3.2.2.1 Experimental conditions 77
3.2.2.2 V_T and W_{fin} dependence 78
3.2.2.3 Device performance 78
3.2.2.4 Advantages 80
3.2.2.5 Limitations 81
3.2.3 Metal/Oxide Interface Modification 81

3.2.3.1 Interface dipole model: introduction 81
3.2.3.2 Implantation-based interface modification 82
3.2.3.3 Gate dielectric nitridation 86
3.2.3.4 Dielectric capping layers 91
3.2.4 Metal Gate Modification 105
3.2.4.1 Metal-inserted capping layers 105
3.2.4.2 Metal thickness-induced V_{fb} shift 110
3.3 Flat Band Voltage Extraction in SOI MuGFETs 117
3.3.1 Work Function Assessment on MOS Structures 118
3.3.1.1 Internal photoemission method 118
3.3.1.2 Flat-band voltage vs. EOT method 119
3.3.1.3 Fowler–Nordheim transition-based method 122
3.3.1.4 Band alignment measurement 123
3.3.2 EVB Tunneling and Band Alignment (nFETs) 124
3.3.2.1 EVB tunneling-based metric: definition 124
3.3.2.2 Metric independence on EOT 127
3.3.2.3 Application to n-MOSFETs 127
3.3.2.4 Extension to p-MOSFETs 128
3.3.2.5 Limitations 130
3.3.3 Gate Leakage Derivative-Based Method 130
3.3.3.1 Band alignment and metric definition 130
3.3.3.2 Comparison with the EVB tunneling-defined method 131
3.3.4 The Fully Depleted Floating Body MuGFET Case 133
3.3.4.1 Framework and constraints 133
3.3.4.2 Flat band voltage extraction 134
3.3.4.3 Limitations 136

4 Doping, Contact and Strain Architectures for Highly Scaled FinFETs **149**
Robert Lander
4.1 Introduction 149

4.1.1 Scaling Issues for Planar CMOS Junctions 150
4.1.2 The FinFET Architecture 152
4.1.3 Performance-Leakage Trade-Offs for Fully Depleted FinFETs 153
4.2 FinFET Device Process Sequence 157
4.3 Extension and Halo Formation 158
4.3.1 Pitch Constraints and Conformal Doping for Extensions 159
4.3.2 Dopant Incorporation by Ion Implantation 161
4.3.3 Alternatives to Ion Implantation 162
4.3.3.1 Plasma doping 162
4.3.3.2 Vapor phase doping 162
4.3.3.3 Epi tip 163
4.3.4 Dopant Retention 163
4.3.5 Dopant Activation 164
4.4 Spacer Formation 168
4.5 Selective Epitaxial Growth, HDD and Salicidation 170
4.5.1 Self-Aligned Silicidation 170
4.5.2 The Doping-Less Transistor? 173
4.5.3 Selective Epitaxial Growth 173
4.5.4 Highly Doped Drain Formation 176
4.6 Channel Strain 176

II. Circuit-Related Aspects

5 Variability and Its Implications for FinFET SRAM 185
Emanuele Baravelli, Luca De Marchi, and Nicolò Speciale
5.1 Introduction 186
5.2 Modeling Variation Sources at the Physical Level 190
5.2.1 LER Metrology 191
5.2.2 TCAD Representation of LER 193
5.3 Impact of Variability at the Device Level 194
5.3.1 Simulation Approach 194
5.3.2 Assessment of LER Contributions to Electrical Fluctuations 197
5.3.3 Correlation Analysis and Comparison of LER Simulation Approaches 200
5.3.3.1 Correlation study 200

5.3.3.2 Exploiting correlations 204
5.3.4 Impact of FinFET Design on LER-Induced Variability 206
5.3.4.1 Number of fins, crystal orientation and WF engineering 207
5.3.4.2 Doping profiles and role of the extensions 208
5.4 Impact of Variability at the Circuit Level 214
5.4.1 Simulation Approach and SRAM Stability Metrics 215
5.4.2 FinFET-Based SRAM Design 217
5.4.3 Hold, Read and Write Operating Conditions 219
5.4.4 SRAM Stability vs. Cell Sizing 220
5.4.5 SRAM Stability vs. Crystal Orientation 222
5.4.6 SRAM Stability vs. Gate Stack 223
5.5 Conclusions 225

6 Specific Features of MuGFETs at High Temperatures over a Wide Frequency Range 233
Valeriya Kilchytska, Jean-Pierre Raskin, and Denis Flandre
6.1 Introduction 233
6.2 Devices, Measurements and Simulation Details 234
6.3 Threshold Voltage 236
6.4 Subthreshold Slope 240
6.5 On-to-Off Current Ratio, I_{on}/I_{off} 246
6.6 Analog and RF Applications 248
6.6.1 Maximum Transconductance-to-Drain Current Ratio, $G_m/I_{d\,max}$ 248
6.6.2 G_m/I_d, Early Voltage and Intrinsic Gain 249
6.6.3 Transconductance Maximum, $G_{m\,max}$ 252
6.6.4 f_T, f_{max} 256
6.7 Conclusions 256

7 ESD Protection in FinFET Technology 261
Steven Thijs
7.1 Introduction 261
7.2 Brief Introduction to ESD 262

7.2.1 Basic ESD Protection Devices 264
7.2.2 Transmission Line Pulsing (TLP) Measurements 266
7.3 Normalization Methodology 267
7.4 Geometrical Dependencies 269
7.4.1 MOS Devices — Parasitic Bipolar Mode 269
7.4.1.1 Gate length dependence 271
7.4.1.2 Fin width dependence 277
7.4.1.3 Number of fins dependence 282
7.4.2 Gated Diodes 285
7.4.2.1 Gate length dependence 286
7.4.2.2 Fin width dependence 287
7.5 Process Technology Dependencies 288
7.5.1 Selective Epitaxial Growth 288
7.5.2 Silicide Blocking 292
7.5.3 Strain 294
7.6 Conclusions 297

III. Exploratory Devices and Characterization Tools

8 The Junctionless Nanowire Transistor 303
Bart Sorée, Anh-Tuan Pham, Dries Sels, and Wim Magnus
8.1 Introduction 304
8.2 Basic Working Principles of the Junctionless Nanowire Transistor 307
8.3 Analytical Model for Long and Thick Nanowires 310
8.3.1 The Abrupt Depletion Approximation 310
8.3.2 The Gradual Channel Approximation: Current Above Threshold 312
8.3.2.1 Flatband condition: $V_G = 0$ 314
8.3.2.2 Depletion: $V_G < 0$ 315
8.3.3 Subthreshold Current 315
8.3.4 Discussion 316
8.4 Low-Field Mobility Modeling for Long Thin Junctionless Nanowires 318
8.4.1 Quantum Mechanical Electronic Structure of the Junctionless Nanowire 319

8.4.1.1 Flatband condition 320
8.4.1.2 Full depletion or pinch-off condition 322
8.4.2 Low Field Mobility and Scattering Mechanisms 323
8.5 Ballistic Transport in Ultrashort Thin Junctionless Nanowires 325
8.5.1 Schrödinger–Poisson Problem 325
8.5.2 Equivalence of the Junctionless (Pinch-Off) and Inversion Mode MOSFET Nanowire 327
8.6 Advanced Transport Modelling of the Junctionless Nanowire Transistor 330
8.6.1 The Poisson–Schrödinger Problem 330
8.6.2 The Boltzmann Transport Equation 332
8.6.3 Results 333

9 The Variational Principle: A Valuable Ally Assisting the Self-Consistent Solution of Poisson's Equation and Semi-Classical Transport Equations 339
Wim Magnus, Hamilton Carrillo-Nuñez, and Bart Sorée
9.1 Introduction 340
9.2 The Electromagnetic Field: Lagrangian and Action 342
9.3 The Principle of Least Action for Self-Consistent Solutions 343
9.4 Ballistic Current in a Si Nanowire Transistor 346
9.4.1 Hamiltonian and Electronic Structure 347
9.4.2 Distribution Function, Kinetic and Constitutive Equations 349
9.4.3 Action Functional and Numerical Algorithm 351
9.4.4 Some Results 354
9.5 Outlook 357

10 New Tools for the Direct Characterisation of FinFETS 361
G. C. Tettamanzi, A. Paul, S. Lee, G. Klimeck, and S. Rogge
10.1 Introduction 361
10.2 Transport in Doped N-FinFETs 362
10.2.1 Thermionic Emission in Doped FinFET Devices 363

10.2.2 Analysis of the Thermionic Regime (High Temperatures) 365
10.2.3 Analysis of the Coulomb Blockade Regime (Low Temperatures) 365
10.2.4 Interpretation of the Results 367
10.2.5 The Corner Effect 368
10.2.6 Temperature Dependence of the Conductance Peaks 368
10.2.7 Conclusion 369
10.3 Transport in Undoped N-FinFETs 369
10.3.1 Introduction to Transport in Undoped Devices 370
10.3.2 Experimental Results 370
10.3.3 Evolution of the Barrier Height with Gate Voltage 372
10.3.3.1 Capacitive coupling 372
10.3.4 Evolution of the Active Cross Section with Gate Voltage 374
10.3.5 Comparison with Simulation 375
10.3.6 Conclusion 377
10.4 Interface Trap Density Metrology of Undoped N-FinFETs 377
10.4.1 Introduction 377
10.4.2 Aim 379
10.4.3 New Implementation of Interface Trap Metrology 380
10.4.4 Device and Experimental Details 380
10.4.5 Modeling Approach 381
10.4.6 Extraction of Barrier Height and the Active Cross Area Section 382
10.4.7 Trap Extraction Methods 383
10.4.7.1 Method I: D_{it} from active area 384
10.4.7.2 Method II: D_{it} from barrier control 385
10.4.7.3 Limitations of the methods 387
10.4.8 Results and Discussion 387
10.4.8.1 Temperature dependence of the barrier height 387

10.4.8.2 Evolution of the barrier height and of the active cross-section area with V_G 389
10.4.8.3 Trap density evaluation 390
10.4.8.4 Discussion of the two methods and D_{it} trends 393
10.4.9 Current Distribution 394
10.4.10 Conclusion 395
10.5 Final Conclusions 396

11 Dopant Metrology in Advanced FinFETs 399
G. Lansbergen, R. Rahman, G. C. Tettamanzi, J. Verduijn, L. C. L. Hollenberg, G. Klimeck, and S. Rogge
11.1 Introduction 399
11.2 Recent Progress in Donor Spectroscopy 400
11.3 Transport-Based Dopant Metrology in Advanced FinFETS 401
11.4 Devices 402
11.5 Results 408
11.6 Conclusions 409

Index 413

Preface

In 1965, Gordon Moore published his legendary paper "Cramming more components onto integrated circuits." In this paper, he described that the number of components in integrated circuits had doubled every year since the invention of the integrated circuit in 1958 until 1965 and that this trend would continue for at least 10 more years. Now, almost five decades later, industry is still following Moore's law, even though its end has been predicted on many occasions and even by Moore himself.

Indeed, one needs to point out that since the development of the 130 nm technology node, it has become more and more difficult to scale down the traditional MOSFET structure in order to keep up with the pace of Moore's law. Especially in the last decade, many innovations such as high-k/metal gate and strain engineering have been introduced to ensure the required performance improvement with every new technology node. However, these material innovations are not enough to control the ever-increasing off-state leakage problem in these advanced devices. New device architectures such as multi-gate devices have emerged as a means to solve this issue by increasing the gate control through geometry. Although proposed already in the beginning of the 1980s, multi-gate devices (Delta FET, FinFET, tri-gate, etc.) and more generally fully depleted transistors have long been considered the exotic devices that somehow were no real contenders to replace the planar bulk MOSFET. With Intel's announcement to introduce the tri-gate architecture on bulk substrates at the 22 nm technology node, a new era of MOSFET scaling arrived. It is expected that more companies will follow and introduce multi-gate devices at future technology nodes.

This book tries to give the reader an insight into the theory, technology, and circuit aspects of FinFET-based multi-gate transistors. It also goes one step further and extends the scope to nanowires and derived device architectures such as the junctionless nanowire FET. Further, some of the chapters discuss the new characterization and mathematical tools to predict the behavior of nanoscale structures.

As such, the book is divided into three main parts with a total of 11 chapters, each written by experts in the field:

Part I: Integration of Multi-Gate Devices (FinFET)

Chapter 1, "Introduction to Multi-Gate Devices and Integration Challenges," by Nadine Collaert, gives an overall introduction to multi-gate devices. It briefly reviews the history of multi-gate devices and discusses their specific advantages over standard bulk devices. Although the integration of these devices is very similar to their planar counterparts, a number of integration challenges are highlighted in this chapter.

Chapter 2, "Dry Etching Patterning Requirements for Multi-Gate Devices," by Efraín Altamirano-Sánchez, Tom Vandeweyer, Marc Demand, and Werner Boullart, describes the challenges of patterning high-density FinFET devices for the 22 nm technology node and beyond. Apart from the 193 nm lithography-based fin patterning, the use of full-field extreme ultraviolet (EUV) lithography is addressed in this chapter.

Chapter 3, "High-k Dielectrics and Metal Gate Electrodes on SOI MuGFETs," by Isabelle Ferain, covers the processing of high-k dielectrics/metal gate electrodes on fully depleted SOI MuGFETs or finFETs. In the second section of this chapter, several methods used for controlling and tuning the work function in MuGFETs with metal gates are described.

Chapter 4, "Doping, Contact and Strain Architectures for Highly Scaled finFETs" by Rob Lander, tackles one of the most important integration challenges of FinFET-based devices and thin Si film devices: reduction of the parasitic source/drain resistance. Next to that, more insight is given into strain engineering techniques in multi-gate devices.

Part II: Circuit-Related Aspects

Chapter 5, “Variability and Its Implications for FinFET SRAM,” by Emanuele Baravelli, Luca De Marchi, and Nicolò Speciale, discusses physical-level models for fin and gate line-edge roughness (LER) that can be applied to estimate their impact on the FinFET electrical performance. Six-transistor (6T) SRAM is used as a benchmark to evaluate the impact of line-edge roughness at the circuit level.

Chapter 6, “Specific Features of MuGFETs at High Temperatures over a Wide Frequency Range,” by Valeriya Kilchytska, Jean-Pierre Raskin, and Denis Flandre, focuses on the high-temperature behavior of SOI-based FinFET devices with a specific focus on analog and RF applications. Although FinFETs show excellent short-channel behavior, it is not clear if they maintain their performance advantages at high temperatures. Some particular features of the high-temperature behavior of advanced FinFETs are highlighted in this chapter.

Chapter 7, “ESD Protection in FinFET Technology,” by Steven Thijs, deals with the Electro-Static Discharge (ESD) robustness of multi-gate architectures. Especially, the early FinFET devices showed very low ESD robustness, which demonstrated the need of considering ESD already in a very early technology development phase. The impact of the different geometrical parameters and technology options is the focus of this chapter.

Part III: Exploratory Devices and Characterization Tools

Chapter 8, “The Junctionless Nanowire Transistor” by Bart Sorée, Ahn-Tuan Pham, Dries Sels, and Wim Magnus, introduces the junctionless nanowire transistor as an alternative device concept to the inversion mode nanowire MOSFET. An analytical model is used to describe the basic working principle. Furthermore, the impact of scaling down both the wire radius and the gate length is addressed in this chapter. Finally, an advanced transport model is used to investigate the impact of strain on the short-channel junctionless nanowire FET.

Chapter 9, "The Variational Principle: A Valuable Ally Assisting the Self-Consistent Solution of Poisson's Equation and Semi-Classical Transport Equations," by Wim Magnus, Hamilton Carrillo-Nuñez, and Bart Sorée, attempts to give the reader some insight into the increasing mathematical complexity that is encountered when nanoscale devices are to be modeled with acceptable accuracy. Specifically, the variational principle is explored as a numerical tool to self-consistently solve Poisson's equation and a set of semi-classical transport equations to describe transport in nanoscale structures.

Chapter 10, "New Tools for the Direct Characterisation of FinFETs," by G. C. Tettamanzi, A. Paul, S. Lee, G. Klimeck, and S. Rogge, discusses how classical transport theories such as the thermionic emission in combination with state-of-the-art tight binding simulations can be used as a powerful tool for the study of the complex transport mechanisms in FinFETs.

Chapter 11: "Dopant Metrology in Advanced FinFETs," by G. Lansbergen, R. Rahman, G. C. Tettamanzi, J. Verduijn, L. C. L. Hollenberg, G. Klimeck, and S. Rogge, describes a new approach to atomistic impurity metrology. The method offers opportunities for non-invasive characterization down to the level of a single donor and could be a future tool in the guidance of device processing.

Finally, I would like to thank all the authors for making this book a diverse yet comprehensive text in which different aspects of nanoscale devices are addressed. Many thanks as well to everyone who indirectly contributed to this work. In particular, I would like to thank my husband, Gunther, and my children, Michiel and Karen, for their continuous support.

Nadine Collaert
July 2012