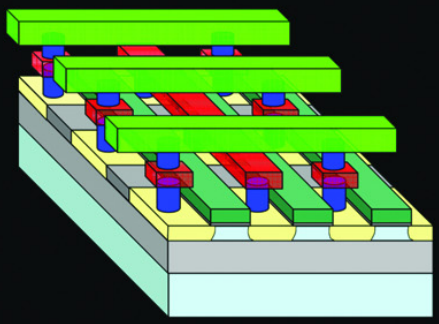
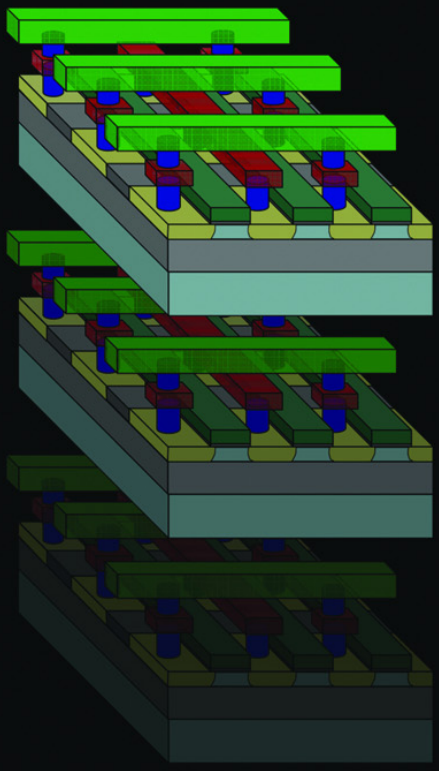
Takashi Ohsawa
Takeshi Hamamoto



a Novel Capacitor-less DRAM Cell

FLOATING BODY CELL



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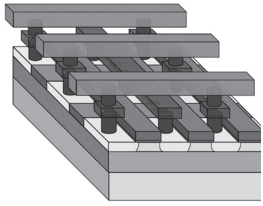

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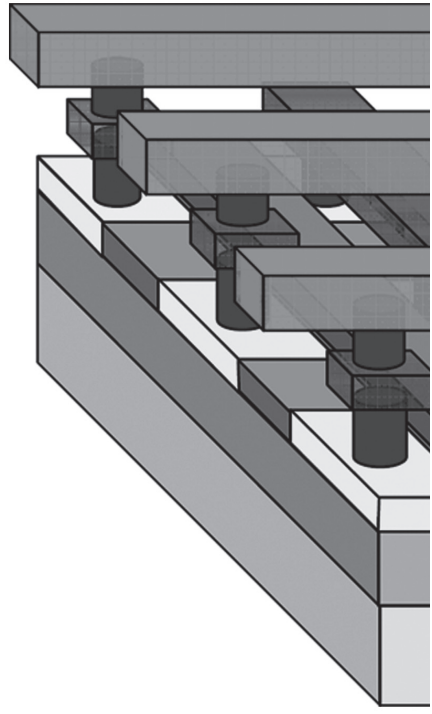

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Contents

Preface

Floating body cell (FBC) is one of the simplest semiconductor memory cells ever proposed, which consists of just a single metal–oxide–semiconductor field-effect transistor (MOSFET) with its body floating. The flash memory cell also consists of a single MOSFET having a floating gate between the gate and the channel. And the both cells rely on a very similar data writing mechanism, i.e., they change the threshold voltage of a MOSFET as a means of memorizing data; the flash cell does it through electrical charges stored in the floating gate, and FBC does it through those stored in the floating body. However, the mere difference in data storage node in a MOSFET makes the flash a non-volatile data storage memory and FBC a volatile random access memory (RAM).

Though the idea of storing data in a floating body of a MOSFET is rather old, the FBC research and development have become especially active since the year 2000 when a useful selective write method by controlling the gate and the drain voltages was invented. FBC consists of a single-transistor cell structure on silicon-on-insulator (SOI) without a capacitor which is used for storing data in the conventional one-transistor and one-capacitor (1T-1C) dynamic random access memory (DRAM). The cell size of FBC is about a half of the conventional DRAM cell. The process to fabricate FBC is almost compatible with the standard CMOS one. These features are attractive especially for embedded memories, for a memory with density larger than the DRAM can be implemented into logic LSIs as freely as many other standard libraries just like the static random access memory (SRAM) without suffering from the difference in process between making the logic transistors and the FBC cells. Furthermore, it can even break through the scaling problems the present-day DRAM is struggling to surmount, because the scaling of FBC with no explicit capacitor to store data is much easier than the DRAM cell.

Many efforts have been made and are still under way for FBC to be phased into real memory products of embedded memory macros and of stand-alone memories alike in a circumstance where the conventional 1T-1C DRAM is suffering from being scaled further. In some cases, the SOI substrate which FBC is necessary to be built on became a bottleneck from a chip cost point of view. In other cases, the data retention time which is shorter than that of the 1T-1C DRAM cell became a showstopper of the project for implementing the small and easy-to-make cell into a stand-alone memory. However, recent proposals of new FBC structures permit the cells to be built on bulk silicon substrate. A new report encourages further efforts to optimize the device structures for the retention time to meet the stand-alone DRAM specifications. Furthermore, the autonomous refresh, an FBC-

specific refresh operation, has been shown to contribute to improving the data retention characteristics, if successfully applied.

This monograph describes a broad spectrum of FBC technologies from the basic principles to its memory design practices, providing a comprehensive summary of the FBC process, devices, circuits, and memory designs. In Chapter 1, the 1T-1C DRAM cell technologies are briefly reviewed with their difficulties in scaling remarked, followed by a short history of capacitorless DRAM cells. In Chapter 2, the concept and the operational principles of FBC is explained with TCAD simulation results which verify the principles. The write selectivity is explained in detail in relation to bit line disturb. A comprehensive summary of write and read methods for FBC is given. In Chapter 3, the mechanism of generating the signal of FBC is analyzed and the signal-to-noise ratios (SNRs) are defined with their criteria for achieving a high-density memory estimated theoretically. In Chapter 4, a 128 Mb memory using FBC is introduced with various data shown for verifying the prediction by the theories. The experimental data on retention time are also presented including its degradation by the bit line disturb. In Chapter 5, the scaling of FBC is discussed. A scaling law in which the SNR is kept constant is shown to hold by TCAD Monte Carlo simulations. In Chapter 6, cell array architectures and sense amplifier designs are explained by comparing the two array architectures, the twin cell and the single cell schemes. A useful dummy cell system to help enhance the chip yield is explained with simulated and experimental data. An attractive array architecture specific to FBC is presented which mitigates inter bit line coupling noise without performance degradation. In Chapter 7, two design practices are discussed and compared; one is a twin-cell-based high-speed embedded memory and the other is a single-cell-based high-density memory. The unique autonomous refresh which can make all cells in an array refreshed at once is explained in detail. As a special example of the autonomous refresh, it is theoretically predicted that FBC can be an SRAM cell if the gate direct tunneling current is used to extract holes from the body with the impact ionization current combined to realize two stably stationary points in retaining data. In Chapter 8, past activities in FBC technology research and development are summarized comprehensively, followed by categorizing them into several high-potential variations. Finally, future directions of FBC technologies are discussed.

Senior undergraduate and graduate students in electrical engineering and microelectronics who are learning SOI technologies will grasp many practical aspects realized in electrical characteristics of a floating body MOSFET through understanding the FBC's operational principles and features described in this book. It also provides memory design practices in device and circuits, which will be useful for engineers and scientists involved in research and development of materials, process, device, and circuits for emerging memories. The device or circuit engineers who are

striving to make FBC usable in a real memory product will understand this particular cell's design points along with its potentials and constraints. We hope that this book will help contribute to a possible breakthrough to make the emerging memory cell be a reality.

Many colleagues we worked with have contributed to the contents of this book. We would like to take this opportunity to thank them all for their contributions to the fruitful results which have grown the FBC technology as is today and is still in progress. We are quite indebted to the following individuals for process, designs, simulations, experiments, measurements, tests, and supports: Nobutoshi Aoki, Yoshiaki Asao, Toshiyuki Enda, Shuso Fujii, Katsuyuki Fujita, Ryo Fukuda, Yoshiaki Fukuzumi, Hironobu Furuhashi, Tohru Furuyama, Kosuke Hatsuda, Tomoki Higashi, Fumio Horiguchi, Tamio Ikehashi, Kazumi Inoh, Hidemi Ishiuchi, Yoshihisa Iwata, Yasuyuki Kajitani, Takeshi Kajiyama, Shigeru Kawanaka, Yusuke Kohyama, Naoki Kusunoki, Fumiyoshi Matsuoka, Yoshihiro Minami, Mutsuo Morikado, Hiroomi Nakajima, Akihiro Nitayama, Yukihito Oowaki, Tomoaki Shino, Kazumasa Sunouchi, Hiroyoshi Tanimoto, Testunori Wada, Shigeyoshi Watanabe, Yohji Watanabe, Takashi Yamada, and Makoto Yoshimi.

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